

Bennett James

bennett-james.com | bennett@jamesotw.com | 704.320.8751

EDUCATION

NC STATE UNIVERSITY

BS IN COMPUTER ENGINEERING

May 2020

GPA: 3.602 | Magna Cum Laude

LINKS

LinkedIn:// [bennett-james](#)

YouTube:// [Bennett James](#)

RELEVANT COURSES

GRADUATE COURSES

ECE560 - Embedded Systems Design

ECE561 - Embedded Systems Optimization

ECE563 - Micro-architecture

ECE564 - FPGA/ASIC design w/ Verilog

ECE592 - Python in Engineering

UNDERGRADUATE COURSES

ECE302 - Microelectronics

ECE306 - Intro to Embedded Systems

ECE309 - Data Structures and OOP

ECE310 - Complex Digital Systems

ECE492 - Java

SKILLS

PROGRAMMING

Proficient:

Verilog • C • C++ • Embedded C

Familiar:

Python • Java • Assembly • SQL

OTHER SKILLS

Embedded Systems Design • Embedded

Systems Optimization • RTOS • ARM

Cortex Processors • FPGA Design and

Simulation (ModelSim) • Synthesizing

FPGAs (Synopsys) • MIPS Pipelining •

BFSK • RSLogix • FactoryTalk • PLC

Ladder Logic

AWARDS

Dean's List (x6)

Simon Brown Woolard Scholarship - 2018

US Marine Corp Distinguished Athlete

Award - 2016

EXPERIENCE

ROVISYS BUILDING TECHNOLOGIES | SYSTEMS INTERN

May 2019 - Aug 2019 | Holly Springs, NC & Charleston, SC

- Designed HMI for a large data center to show and maintain precise measurements of all necessary specifications.
- Programmed PLCs using Ladder Logic.
- Commissioned systems to be turned over to client.

PROJECTS

IOT ENABLED MINIATURE CAR | ECE306

Jan 2019 - Apr 2019

Small vehicle with capabilities to navigate through a course following a black line or act on directional commands from a user.

G(T) GATE FOR AN LSTM | ECE564

Sep 2019 - Nov 2019

Designed, implemented, and synthesized a g(t) gate within an LSTM using Verilog and Synopsys.

ACCELEROMETER OPTIMIZATION | ECE560

Sep 2019 - Oct 2020

Using the FRDM-KL25Z's onboard accelerometer, optimized code for accelerometer updates.

TOUCHSCREEN DISPLAY SHOWING LED CURRENT | ECE560

Nov 2019 - Dec 2019

Shared ADC between the Buck LED and touchscreen using message queues. Then added code to draw current from buck LED.

5 STAGE MIPS PIPELINE | ECE563

Jan 2020 - Feb 2020

Designed 5 stage pipeline in C++ designing the functions for handling asm files to read and perform respective instructions.

GPS OPTICAL COMMUNICATIONS | ECE484/485 SENIOR DESIGN

Aug 2019 - Apr 2020

Implemented a method for communicating GPS data using optical means. Personal responsibilities included modulating the data and designing the enclosure.

SPEED ANALYSIS AND OPTIMIZATION | ECE561

Feb 2020 - Mar 2020

Reduced sample size of code to read and display images from a micro SD.

DYNAMIC SCHEDULING PROCESSOR | ECE563

Mar 2020 - Apr 2020

Implemented Tomasulo's algorithm using reorder buffers, reservations stations, and execution units.

MEMORY SIZE OPTIMIZATION | ECE561

Apr 2020

Optimize accelerometer code by reducing stack size and frame of several functions.

CACHE | ECE563

Aug 2019 - Apr 2020

Designed cache and implemented with mips pipeline project to perform vector addition and matrix multiplication.